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INC. Commercial

PEEL™22CV10A -7/-10/-15/L-15/-25
CMOS Programmable Electrically Erasable Logic Device

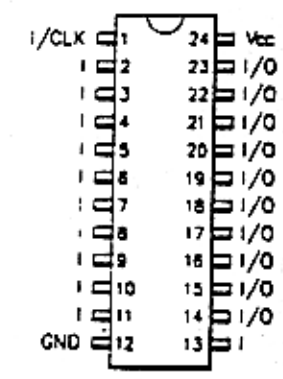
Features

- **High Speed/Low Power**
  - — Speeds ranging from 7ns to 25ns
  - — Power as low as 67mA at 25MHz
- **Electrically Erasable Technology**
  - — Superior factory testing
  - — Reprogrammable in plastic package
  - — Reduces retrofit and development costs
- **Development/Programmer Support**
  - — Third party software and programmers
  - — ICT PLACE Development Software and PDS-3 programmer
- **Architectural Flexibility**
  - — 132 product term X 44 input AND array
  - — Up to 22 inputs and 10 outputs
  - — Up to 12 configurations per macrocell
  - — Synchronous preset, asynchronous clear
  - — Independent output enables
  - — 24-pin DIP, SOIC and 28-pin PLCC packages
- **Application Versatility**
  - — Replaces random logic
  - — Pin and JEDEC compatible with 22V10
  - — Enhanced Architecture fits more logic than ordinary PLDs

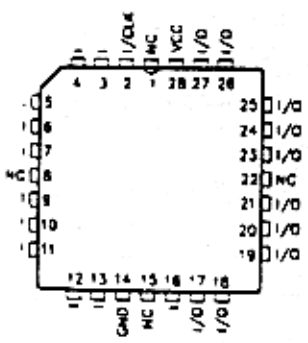
General Description

The PEEL22CV10A is a Programmable Electrically Erasable Logic (PEEL) device providing an attractive alternative to ordinary PLDs. The PEEL22CV10A offers the performance, flexibility, ease of design and production practicality needed by logic designers today. The PEEL22CV10A is available in 24-pin DIP, SOIC and 28-pin PLCC packages with speeds ranging from 7ns to 25ns with power consumption as low as 67mA. EE-Reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-Reprogrammability also improves factory testability thus, assuring the highest quality possible. The PEEL22CV10A is JEDEC file compatible with standard 22V10 PLDs. Eight additional configurations per macrocell (a total of 12) are also available by using the "+" software/programming option (i.e, 22CV10A+). The additional macrocell configurations allow more logic to be put into every design. Development and programming support for the PEEL22CV10A is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

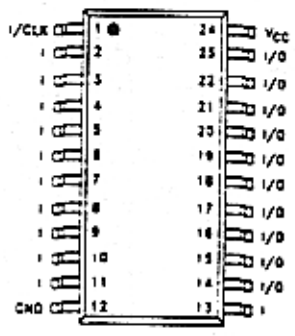
Pin Configuration (Figure 1)



DIP

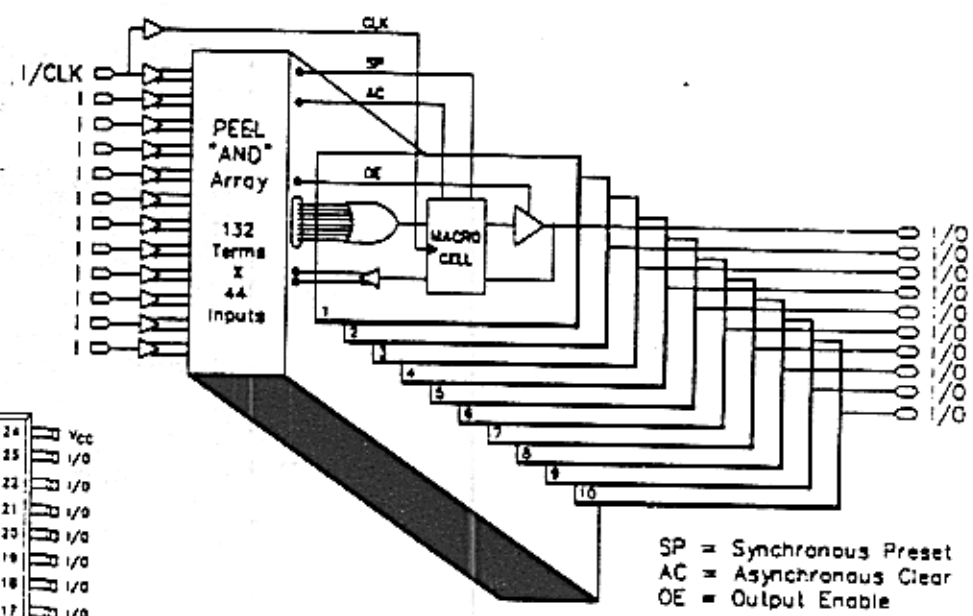


PLCC



SOIC

Block Diagram (Figure 2)



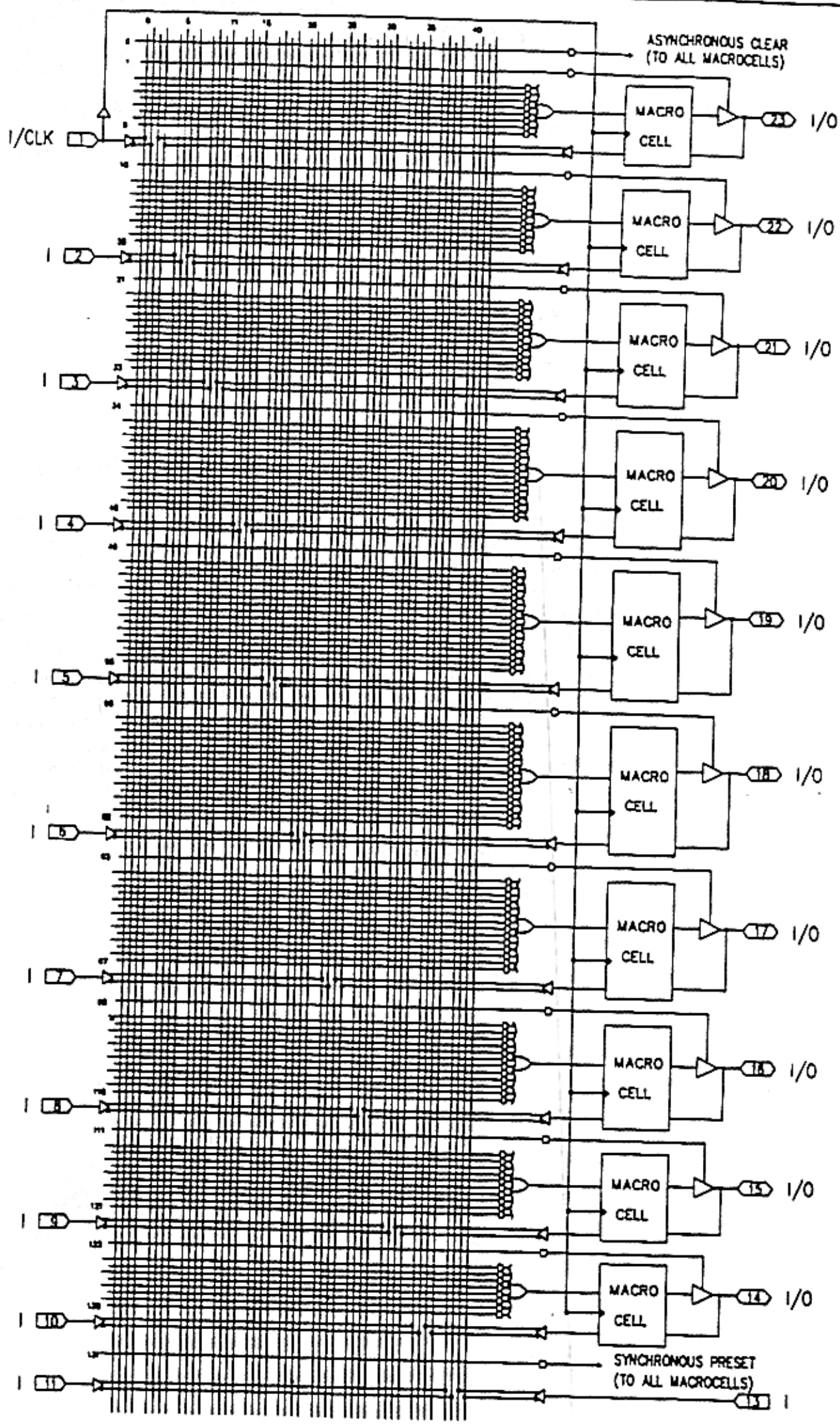


Figure 3. PEEL22CV10A Logic Array Diagram

Function Description

The PEEL22CV10A implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview

The PEEL22CV10A architecture is illustrated in the block diagram of figure 2. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure, the PEEL22CV10A can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is an I/O macrocell which can be independently programmed to one of 4 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions with either active-high or active-low polarity.

AND/OR Logic Array

The programmable AND array of the PEEL22CV10A (shown in figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 Input Lines:

- 24 input lines carry the true and complement of the signals applied to the 12 input pins
- 20 additional lines carry the true and complement values of feedback or input signals from the 10 I/Os

132 product terms:

- 120 product terms (arranged in 2 groups of 8, 10, 12,14, and 16) used to form logical sums
- 10 output enable terms (one for each I/O)
- 1 global synchronous present term
- 1 global asynchronous clear term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term which is connected to both the true and compliment of an input signal will always be FALSE, and thus will not effect the OR function that it drives. When all the connections on a product term are opened, a don't care state exists and that term will always be TRUE.

When programming the PEEL22CV10A, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is then configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program the connections on unused product terms so that they will have no effect on the output function)

Variable Product Term Distribution

The PEEL22CV10A provides 120 product terms to drive the 10 OR functions. These product terms are distributed among the outputs in groups of 8, 10, 12, 14, and 16 to form logical sums (see figure 3). This distribution allows optimum use of device resources.

Programmable I/O Macrocell

The output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL22CV10A to the precise requirements of their designs.

Macrocell Architecture

Each I/O macrocell, as shown in figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell is determined by the two EEPROM bits controlling these multiplexers (refer to table 1). These bits determine output polarity and output type (registered or non-registered). Equivalent circuits for the four macrocell configurations are illustrated in figure 5.

Output Type

The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity
Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable
The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select
When configuring an I/O macrocell to implement a registered function (configurations 1 and 2 in Figure 5), the Q output of the flip-flop drives the feedback term. When configuring and I/O mcrocell to implement a combinatorial function (configurations 3 and 4 in Figure 5), the feedback signal is taken from the I/O pin. In this case, the pin can be used as a dedicated input or a bi-directionl I/O. (Refer also to Table 1)

Additional Macro Cell Configurations
Besides the standard four-configuration macro cell shown in figure 5, each PEEL22CV10A provides an additional eight configurations that can be used to increase design flexibility. The configurations are the same provided by the PEEL18CV8. However, to maintain JEDEC file compatibility with standard 22V10 PLDs the additional configurations can only be utilized by specifying the PEEL22CV10A+ for logic assembly and programming. To reference these additional configurations please refer to the PEEL22CV10A+ specifications at the end of this data sheet.

Design Security
The PEEL22CV10A provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

Signature Word
The signature word feature allows a 24-bit code to be programmed into the PEEL22CV10A if the PEEL22CV10A+ software option is used. The code can be read back even after the security bit has been set. The signature word can be used to identify the pattern programmed into the device or to record the design revision, etc.

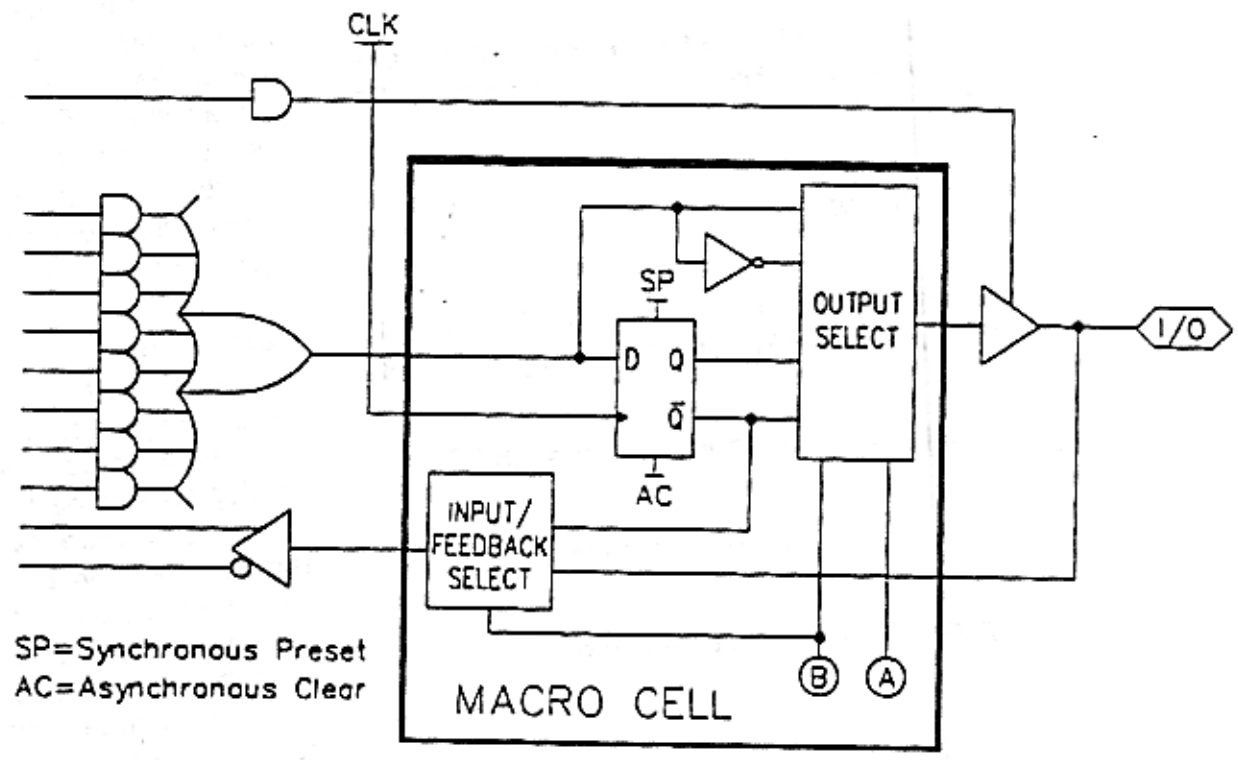


Figure 4. Block Diagram of the PEEL22CV10A I/O Macrocell

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin [3]	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges[2]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial [2]	4.75	5.25	V
T_A	Ambient Temperature	Commercial [2]	0	+ 70	°C
T_R	Clock Rise Time	See note 4		20	ns
T_F	Clock Fall Time	See note 4		20	ns
T_{RVCC}	V_{CC} Rise Time	See note 4		250	ms

D.C. Electrical Characteristics

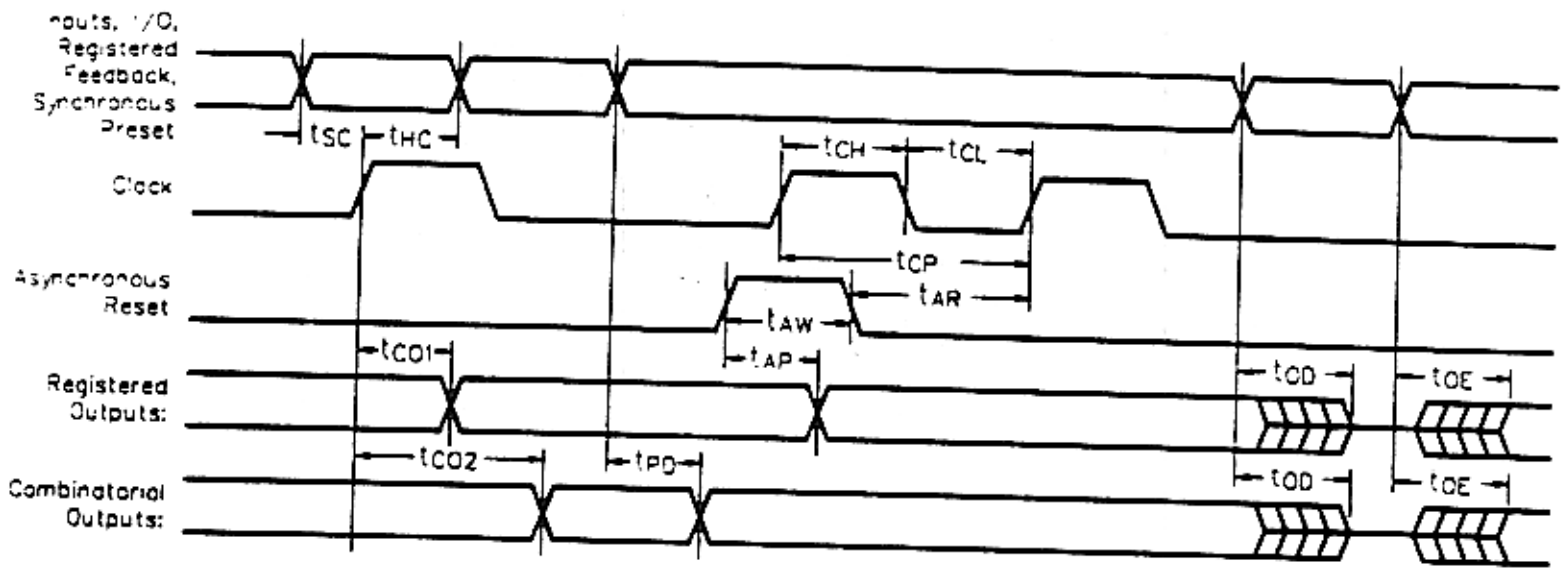
Over the operating range

Symbol	Parameter	Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = − 4.0mA		2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA		V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 16mA			0.5	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA			0.1	V
V_{IH}	Input HIGH Level			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level			− 0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}			±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}			±10	µA
I_{SC}	Output Short Circuit Current	V_{CC}=5V, V_O=0.5V[10], T_A = 25°C		− 30	− 135	mA
I_{CC}[11]	V_{CC} Current (See CR-1 for typical I_{CC})	V_{IN} = 0V or 3V f = 25MHz All outputs disabled[5]	-7		155	mA
			-10		135	mA
			-15		135	mA
			L-15		75	mA
			-25		67	mA
C_{IN}[8]	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz			6	pF
C_{OUT}[8]	Output Capacitance				12	pF

A.C. Electrical Characteristics Over the Operating Range [9,12]

Symbol	Parameter	-7		-10		-15		L-15		-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input [6] to non-registered output		7.5		10		15		15		25	ns
t_{OE}	Input [6] to output enable [7]		7.5		10		15		15		25	ns
t_{OD}	Input [6] to output disable [7]		7.5		10		15		15		25	ns
t_{CO1}	Clock to output		5.5		6		8		10		15	ns
t_{CO2}	Clock to comb. output delay via internal registered feedback		10		12		17		19		35	ns
t_{CF}	Clock to Feedback		3.5		4		5		6		9	ns
t_{SC}	Input [6] or feedback setup to clock	3		5		8		10		15		ns
t_{HC}	Input [6] hold after clock	0		0		0		0		0		ns
t_{CL},t_{CH}	Clock low time, clock high time [9]	3		4		6		7.5		13		ns
t_{CP}	Min clock period Ext (t_{SC} + t_{CO1})	8.5		11		18		20		30		ns
f_{max1}	Internal Feedback (1/t_{SC}+t_{CF}) [13]	142		111		76.9		62.5		41.6		MHz
f_{max2}	External Feedback(1/t_{CP}) [13]	117		90.9		62.5		50		33.3		MHz
f_{max3}	No Feedback (1/t_{CL}+t_{CH}) [13]	166		125		83.3		66.7		38.4		MHz
t_{AW}	Asynchronous Reset pulse width	7.5		10		15		15		25		ns
t_{AP}	Input [6] to Asynchronous Reset		7.5		10		15		18		25	ns
t_{AR}	Asynchronous Reset recovery time		7.5		10		15		18		25	ns
t_{RESET}	Power-on reset time for registers in clear state		5		5		5		5		5	µs

Switching Waveforms



1. Minimum DC input is – 0.5V, however inputs may undershoot to – 2.0V for periods less than 20ns.
2. Contact ICT for other operating ranges.
3. V_I and V_O are not specified for program/verify operation.
4. Test points for Clock and V_{CC} in t_R, t_F are referenced at 10% and 90% levels.
5. I/O pins are 0V or 3V.
6. "Input" refers to an Input pin signal.
7. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$; $V_{REF} = V_L$ see test loads at the end of this section.
8. Capacitances are tested on a sample basis.
9. Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
10. Test one output at a time for a duration of less than 1 sec.
11. ICC for a typical application: This parameter is tested with the device programmed as a 10-bit Counter.
12. PEEL Device test loads are specified at the end of this section.
13. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.